VIKRAM SURESHRAO INGOLE

M.E.in Digital Electronics, Gulabrao Maharaj Colony, V.M.V.Road, Amravati 444604. Mobile: 8380008509 Email: <u>vikramingole1@gmail.com</u>

Visit Website: http://fab.academany.org/2020/labs/vigyanashram/students/vikram-ingole/

OBJECTIVE

Seeking a position with an organization where I can contribute my skills for organization's success and synchronize with new technology while being resourceful, innovative and flexible.

SKILL SET

EDA Tools	: Cadence design Software ,Xilinx,	
	MICROWIND, Multisim, Tanner Tools, H-spice,	
	KEIL, ADS, and P-spice.	
Hardware Description Languages:	s: Verilog, VHDL.	
Platforms	: LINUX, Windows.	
Architectures	: μP 8085,	
Assembly Programming	: μP 8085,	
CNC Machine operate	: ShopBot,3D Printing, PCB tracing machine, I engraver, Vinyl cutter	Laser
	EDA Tools Hardware Description Languages Platforms Architectures Assembly Programming CNC Machine operate	 EDA Tools : Cadence design Software ,Xilinx, MICROWIND, Multisim, Tanner Tools, H-spice, KEIL, ADS, and P-spice. Hardware Description Languages: Verilog, VHDL. Platforms : LINUX, Windows. Architectures : μP 8085, Assembly Programming : μP 8085, CNC Machine operate : ShopBot,3D Printing, PCB tracing machine, I engraver ,Vinyl cutter

TECHNICAL EXPERTISE

Electronics design, Computer controlled cutting, 3D printing, PCB designing, Interface and application, Networking and communication, Web development, GIT version control, 2D & 3D designing.

Digital Electronics: Multivalued Logic Design, Microprocessors, Microcontrollers & Interfacing, FPGA Based System Design, Low Power CMOS VLSI Design

ACADEMIC PROFILE

Degree	Board / University	Year	CGPA / Percentage
Fab Academy Graduate	FAB Academy USA,Bostun	2019	-
M.E. [Digital Electronics]	SGBAU, Amravati	2013	69.5%
B.E [Electronics and Telecommunication]	SGBAU, Amravati	2009	70.04%

ACHIEVEMENTS

- > Awarded as **Best paper** in international conference at BDCOE Sevagram.
- > "CMOS, Mixed Signal and Radio Frequency VLSI Design" at PRMIT&R Badnera.
- STTP attended on "Emerging trends in artificial neural network with Matlab" held at G.H.Raisoni College of engineering and management, Amravati.
- > Attended regional seminar on "wireless sensor networks".
- > STTP attended on "Application of Signal Processing: A system Approach".
- > Attended two days workshop on "Cloud Computing".

CURRENT STATUS

• Working as an Assistant Professor at Shri Sant Gajanan Maharaj College of Engineering, Shegaon.

PROJECTS

M.E. Final Year Project

Title: Design and analysis of CMOS Ternary logic gates.

Description: Multiple-valued logic (MVL) has in the last few decades been proposed as a possible substitute of binary logic. While binary logic is limited to only two states, "true" or "false", multiple-valued logic (MVL) can replace these with finitely or infinitely numbers of values. A MVL system is defined as a system operating on a higher radix than two. The devices should be able to switch between the different logical levels, and preferably be less complex than the binary counterparts.

Tool used: ADS

Team Size: 1

B.E. Project

Title: Optimize design of VCO using CMOS technology.

Duration : 4 months

Description : The layout of VCO which is develop by us is modified design of Vco. This modified design is a optimized design for use in industries at 65 nanotechnology in the estimated design, more emphases is given as power dissipation

is low, size of VCO is small, low fabrication cost.

Team Size: 4

MEMBERSHIP:

➤ Associate member of IETE (AMIETE).

➢ Associate member of ISTE (LMISTE).

PUBLICATION:

- "Design of Multiplexer using CMOS TERNARY LOGIC" V.S. Ingole, Prof.V.T.Gaikwad / International Journal of Engineering Research and Applications (IJERA) Vol. 2, Issue 2,Mar-Apr 2012, pp.1591-S.ISSN: 2248-9622.
- "Design of CMOS INVERTER based on TERNARY LOGIC" V.S.Ingole, Prof.V.T.Gaikwad Proceedings of International Conference of 'Benchmarks in Engineering Science and Technology (IC-BEST) 7-8 September 2012.
- "Design of Ternary NAND Gates Using Ternary Transmission Gates" Asst.Prof.V.S.Ingole, Dr.R.M.Deshmukh, International Journal of Pure and Applied Research in Engineering and Technology 29th March 2014.
- "Design and implementation of low power ternary decoder", Asst.Prof.V.S.Ingole, Dr.V.T.Ingole, International Journal of Pure & Applied Research in Engineering & Technology, 2016.
- "Optimization of CMOS devices in multi valued logic decoder" Asst.Prof.Vikram S.Ingole, Prof. Vinay U. Kale, Dr.Vijay.T.Ingole, International Journal of Scientific & Engineering Research, Volume 7, Issue 11, November-2016 1325 ISSN 2229-5518.
- "Design & Implementation of Digital to Digital Converter comprising Binary Logic to Ternary Logic" Vinay U. Kale, Vijay T. Ingole, Vikram S. Ingole, Ashwin K. Thakur, International Journal of Advanced Scientific and Technical Research Issue 7 volume 1, January – February 2017.

List of other Projects:

- Cattle health Monitoring system (<u>http://fab.academany.org/2020/labs/vigyanashram/students/vikram-ingole/</u> assignments/ Final % 20Project.html)
- Title: "Design and Implementation of D flip-flop for maximum performance using CMOS technology" Tool used: Microwind 11.3
- 3) Title: VLSI based low power, high speed flip-flops using submicron CMOS Technology Tool used: Microwind 11.3
- 4) Title "Design and Implementation of Domino Logic Circuit in CMOS".

Tool used: Microwind 11.3

5) Title: Design and Implementation of ternary Logic over Quaternary Logic.

Tool used: Microwind 11.3

- ➢ Hard working and good at team work.
- > Rapid at learning things.

PERSONAL DETAILS

Father name:	Sureshrao B Ingole
Sex:	Male
Marital status:	Single
Nationality:	Indian
Corresponding address:	V.S.Ingole,
	52, Gulabrao Maharaj colony,
	V.M.V. Road,
	Amravati.
Mobile number:	8380008509
Date of birth:	17 th June 1988

DECLARATION:

I hereby declare that the above mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of above mentioned particulars.

Place : Amravati

Vikram S Ingole